

# Development, Analysis and Implementation of Pre-Processing Video Filters

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## Abstract

The usage of video systems in households and industry has increased rapidly over the past few years. The benefits of visual processing, control and inspection have offered great opportunities for real-time video processing systems (RTVPS) for the general public as well as for heavy industries. The high volume market media systems can absorb a great deal of the cost related to the development of standard components, such as Field Programmable Gate Arrays (FPGAs). The development of industrial systems can benefit from this new technology by utilizing these cheap components. In this thesis, examples of video processing algorithms suitable for pre-processing of digital video applicable for both industrial and media usage will be shown. In addition a methodology supporting the designer in implementing memory architectures suitable for such algorithms is presented.

In this thesis two video processing algorithms are presented and described in detail. The common denominator is their utilization of data from temporally adjacent frames in order to be effective, in terms of compression efficiency, and to produce an attractive result for the viewer. However, from the aspect of quality improvement, considerations have to be taken into account in order to enable an actual hardware implementation. Utilizing data from temporally adjacent frames in a real-time data stream is a non-trivial task. From the algorithm designer's view the data dependencies and memory requirements are not in focus, but for the hardware designer they are. Having the right data available at the right time is the only consideration in order to have a functional system.

Present day algorithm and hardware development methods and architectures do not converge into a common design flow, even though this has been attempted. The gap between the algorithm designer and his/her hardware counterpart has to be bridged in order to obtain an efficient and rapid implementation. Methodologies that abstract and reduce the amount of time spent on implementing memory architectures for video processing applications are required. The buffering requirements are often too complex to analyze manually in order to efficiently utilize the resources available in FPGAs.

In this thesis a method for the synthesis and implementation of memory architectures for real-time video processing systems, IMapper, is presented. The architecture supports the implementation of spatio- and temporal video processing algorithms and utilizes methodologies for global optimization of on-fabric available memory resources for FPGAs. This methodology provides an efficient and flexible implementation environment and also offers the benefits of the global optimizations it utilizes