ABSTRACT

The rapid development of digital circuits with high density and frequency motivates power, in addition to area and speed, to become an important parameter in design constraints. Nowadays, the electronic design industry is confronted by increasingly costly package and cooling systems due to power dissipation. Battery-powered portable devices, such as laptops, mobile phones etc., which provide higher computational capacity and support multi-media information transformation, make the original slim power budget a heavier burden. Although synchronous digital design has, over the past few decades, become the industry standard, this new challenge suggests that asynchronous design techniques should now be reconsidered, as they possess the potential for a reduction in power dissipation.

Finite state machine (FSM) partitioning has proved to be effective for power optimization. In this thesis, a mixed synchronous/asynchronous state memory structure in the decomposed FSM is proposed, which results in implementations with low power dissipation and low area overhead. The state memory is composed of the synchronous local state memory and asynchronous global state memory, where the former is used to distinguish the states inside a sub-FSM, and the latter is responsible for controlling sub-FSM communication. Although asynchronous communication mechanism is introduced between sub-FSMs, the input/output behavior of the decomposed FSM is still, cycle by cycle, equal to that of a complete synchronous FSM. The power consumption can be further reduced by using the clock gating technique and low power state assignment.

Based on this mixed synchronous/asynchronous structure an automatic synthesis tool was developed, which accepts a state transition graph (STG) as the input and synthesizable VHDL code as the output. The output can be directly used for synthesis at the gate level by the standard tool. The FSM partitioning algorithm, power and area estimation and trade-off, and state encoding optimization aimed at this specific structure were integrated into the tool. In addition, the input to the tool was also analyzed, and variation coefficient was proposed as an important measure for the quantitative analysis of power-related characteristics of standard benchmark circuits. The effectiveness of the whole procedure was verified through optimization of standard benchmarks where a power reduction of up to 70% has been demonstrated. Moreover, the proposed asynchronous modules implemented in the tool provide a direction on how the asynchronous design can be effectively combined into a largely synchronous environment.